Amendments to the Specification:

Please replace paragraph at page 10 lines 6-14 of the specification with the following amended paragraph:

The decoder circuit 230 also provides command information included in the data structure to a programmable memory controller circuit 240 based on information included with the ~~command~~ command/address field 355. The programmable memory controller circuit 240 provides control signals to the programmable memory 220 to be used in conjunction with the address and/or data provided by the buffer circuit 235 to the programmable memory 220. Accordingly, the address, data, and control signals can perform the transfer of program data from the interface to the programmable memory 220. In some embodiments according to the invention, a read can be performed subsequent to a write to verify that program data was correctly stored within the programmable memory 220.

Please replace paragraph at page 11 lines 11-20 of the specification with the following amended paragraph:

The general operation processor circuit is disabled from accessing the programmable memory until transfer of the data to the programmable memory has been completed (Block 420). Data included within the data field of the data structure is transferred (in the case of a write operation) to the programmable memory (Block 425). A read operation may be performed to determine that the data (Block 425) was correctly written to the programmable memory (Block 430). ~~The general processor operation circuit is enabled to allow access thereof to the programmable memory upon completion of the transfer of the data to the programmable memory (Block 435)~~. The electronic device control circuit is reset to enable operations of the electronic device according to the newly transferred program (Block 440).